Design Guidelines for CompactPCI Hot Swap Control Applications Using the LTC1644

by Andy Gardner

Introduction

The LTC®1644 is designed for CompactPCI™ Hot Swap™ control applications requiring –12V, 5V, 3.3V and 12V supplies (see Figure 1). The LTC1644 also precharges the bus I/O pins during hot insertion and extraction, feeds back the status of the back-end supply voltages with its $\overline{\text{PWRGD}}$ output, and intercepts the PCI_RST# signal on-chip using the $\overline{\text{RESETIN}}$ and $\overline{\text{RESETOUT}}$ pins. There are several important considerations in circuit design and component selection for CompactPCI Hot Swap control applications using the LTC1644.

Long and Medium Power Pin Connections

CompactPCI connectors have both long and medium length GND, 5V, 3.3V and $V_{I/O}$ power pins as well as medium length –12V and 12V power pins. In general, medium length power pins are used for "Back End Power Planes" where the connector pins are isolated from the load by the LTC1644. The long connector pins may be used to provide "Early Power" to loads that require power immediately upon hot insertion without the benefit of

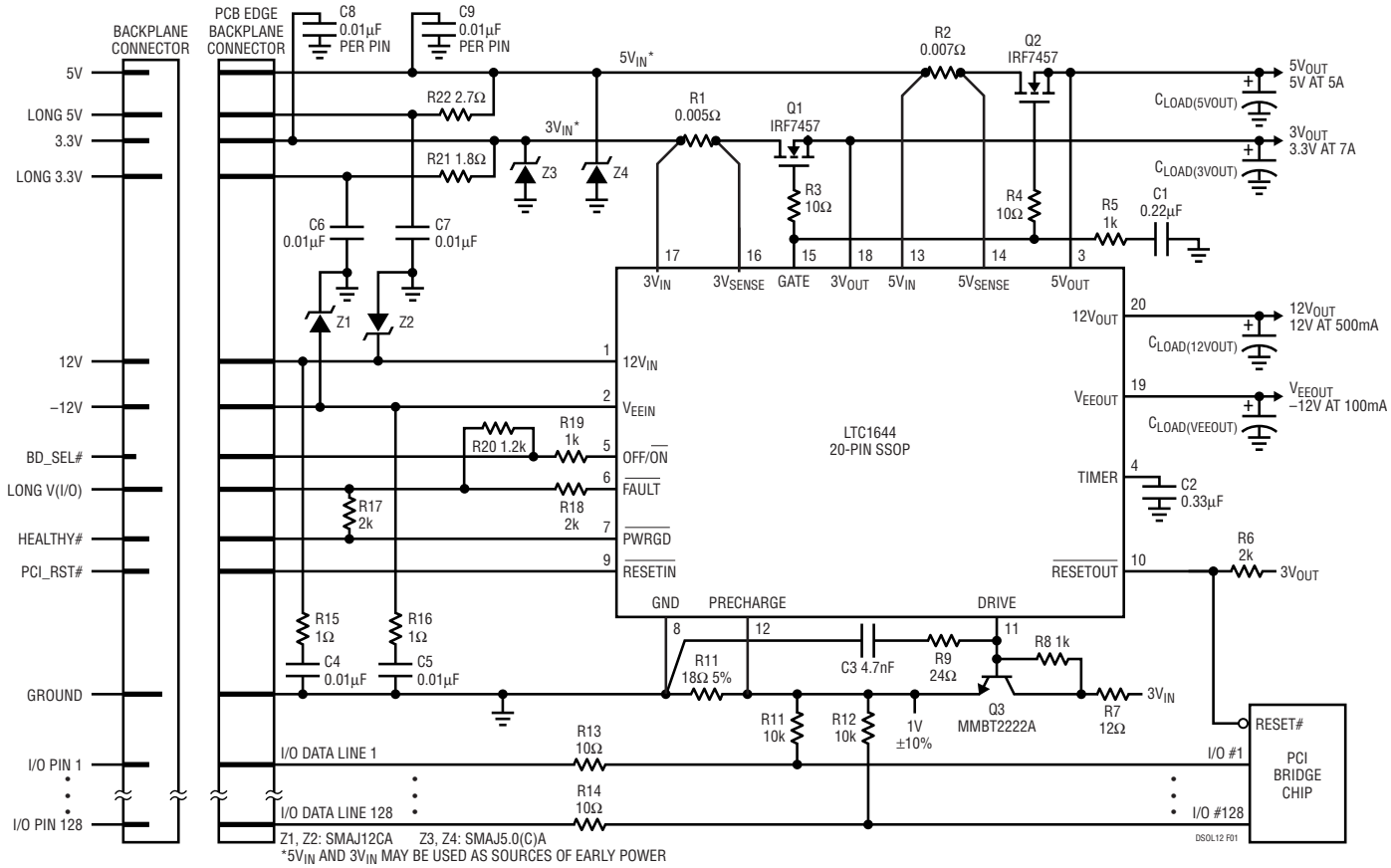

Figure 1. Typical CompactPCI Hot Swap Control Application

active isolation. The LTC1644's PRECHARGE circuitry requires early power from the 5V and 3.3V long connector pins in order to bias the I/O connector pins to 1V before the medium connector pins mate (if precharge is implemented; otherwise, there is no need to provide early power to the LTC1644's $5V_{IN}$ and $3.3V_{IN}$ pins). The long 5V and 3.3V power pins need to be decoupled at the connector by 10nF capacitors (C8 and C9 in Figure 1). Since CompactPCI requires that the current per pin be less than 2A, settling to less than 1A in 100µs, series resistors are used to limit inrush current for each long connector pin (R21 and R22 in Figure 1) that is connected to the $5V_{IN}$ and $3.3V_{IN}$ power planes.

The –12V and 12V medium length power pins connect directly to the LTC1644. Since the potential exists for voltage transients to occur that might exceed the LTC1644's rated absolute maximum voltages, it's necessary to use both R-C snubbers (R15-C4 and R16-C5 in Figure 1) as well as voltage limiters (Z1 and Z2 in Figure 1). Snubbers are series R-C networks connected between the power rail and ground. When combined with the parasitic inductance of the backplane power supply trace, the snubber creates a series R-C-L circuit. The effect of the resistor in this network is to dissipate the energy initially stored in the parasitic inductance during live insertion, thus preventing the resulting voltage transient from exceeding the absolute maximum ratings of the LTC1644's $12V_{IN}$ and V_{EEIN} pins. Voltage limiters also protect against overshoot of voltage transients caused by abrupt changes in load current.

All medium length 5V and 3.3V power pins (even unused power pins) should be decoupled by an average of 10nF of capacitance per pin. Although the 5V and 3.3V medium length connector pins that contact the LTC1644 don't require snubbers, voltage limiters (Z3 and Z4 in Figure 1) are indicated since voltage transients resulting from abrupt changes in load current may also exceed the device's absolute maximum rating.

Precharge Circuit Considerations

Precharge resistors are used to connect the 1V bias voltage to the I/O lines with minimal disturbance. Figure 1 shows the precharge application circuit for 5V signaling. The precharge resistor requirements are more stringent for 3.3V and universal Hot Swap boards. If the total leakage current on the I/O line is less then 2µA, then a 51k resistor should be connected directly from the 1V bias voltage to the I/O line. However, many ICs connected to the I/O lines can have leakage currents up to 10µA. For these applications, a 10k resistor is used but must be disconnected when the board is seated as determined by the state of the BD_SEL# signal. Figure 2 shows a precharge circuit that uses a bus switch to connect the individual 10k precharge resistors to the LTC1644's 1V PRECHARGE pin. The electrical connection is made (bus switches closed) when the voltage on the BD_SEL# pin of the plug-in card is pulled up to $5V_{IN}$, which occurs just after the long pins have made contact. The bus switches are electrically disconnected when the short, BD_SEL# connector pin makes contact and the BD_SEL# voltage drops below 4.4V, thus causing the bus switch $\overline{OE}$ to be pulled high by Q2.

The CompactPCI specification assumes there is a diode clamp to 3.3V on the BD_SEL# pin. If the BD_SEL# pin is driven high, the actual voltage on the pin will be approximately 3.9V. This is above the high TTL threshold of the LTC1644 OFF/$\overline{ON}$ pin, but low enough for Q2 to disable the bus switches and thus disconnect the 10k precharge resistors from the I/O lines. Since the power to the bus switch is derived from an early power plane, a 100Ω resistor should be placed in series with the power supply of the bus switch.

When the plug-in card is removed from the connector, the BD_SEL# connection is broken first and the BD_SEL#

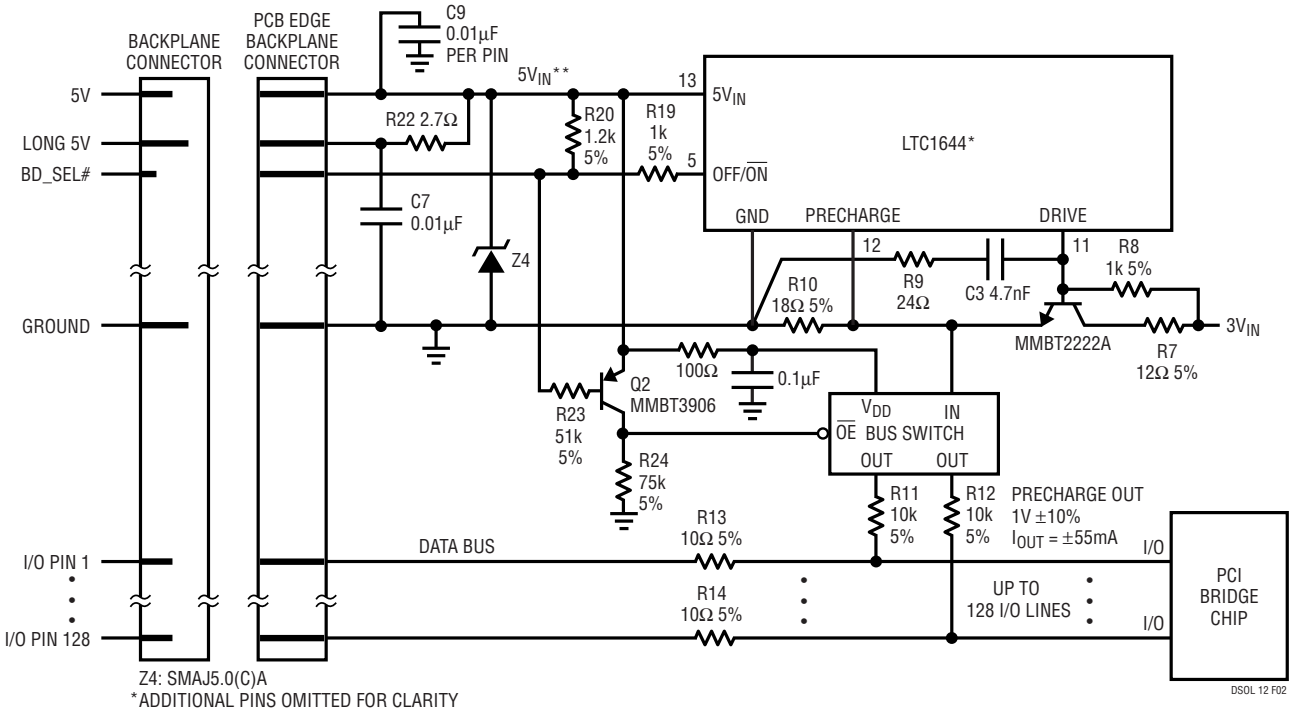

Figure 2. Precharge Bus Switch Application Circuit for 3.3V and Universal Hot Swap Boards

voltage pulls up to $5V_{IN}$. This causes Q2 to turn off, which re-enables the bus switch and the precharge resistors are again connected to the LTC1644 PRECHARGE pin for the remainder of the extraction process.

5V and 3.3V MOSFET Selection

The LTC1644 uses external MOSFETs to limit the 5V and 3.3V supply currents. The following criteria should be used when selecting these MOSFETs:

1. The on resistance should be low enough to prevent an excessive voltage drop across the sense resistor and the series MOSFET at rated load current given the amount of gate to source voltage provided by the LTC1644 (7V for the 5V MOSFET and 8.7V for the 3.3V MOSFET).
2. The drain-to-source breakdown voltage should be high enough for the device to survive overvoltage transients that may occur during fault conditions (the 5V and 3.3V voltage limiters shown in Figure 1 will limit the maximum drain-source voltage seen by these MOSFETs during fault conditions).
3. The MOSFET package must be able to handle the maximum, steady-state power dissipation for the ON state without exceeding the device's rated maximum junction temperature. The MOSFET's steady-state dissipated power can be expressed as:

$$P_{ON} = I_{MAX}^2 \bullet R_{DS(ON)} \quad (1)$$

The increase in steady-state junction-to-ambient temperature is given by:

$$T_J - T_A = P_{ON} \bullet R_{\theta JA} \quad (2)$$

4. The MOSFET package must be able to dissipate the heat resulting from the power pulse during the transition from off to on. A worst-case approximation for the magnitude of the power pulse is:

$$P_{OFF\text{-}ON} < nV_{OUT} \bullet \frac{I_{INRUSH} + I_{LOAD}}{2} \quad (3)$$

where $nV_{OUT} = 5V_{OUT}$ or $3.3V_{OUT}$, I_{INRUSH} is the transient current initially charging the load capacitance and I_{LOAD} is the steady-state load current. The duration, t_{ON}, of the power pulse can be expressed as:

$$t_{ON} = \frac{C_{LOAD} \bullet V_{OUT}}{I_{INRUSH}} \quad (4)$$

5. The MOSFET package must be able to sustain the

maximum pulse power that occurs in the event the LTC1644 attempts to power-up either the 5V or 3.3V back-end supply into a short (see Design Example for sample calculation).

GATE Pin Capacitor Selection

Both the load capacitance and the LTC1644's GATE pin capacitance (C1 in Figure 1) affect the ramp rate of the $5V_{OUT}$ and $3.3V_{OUT}$ voltages. The precise relationship can be expressed as:

$$\frac{dV_{nVOUT}}{dt} = \frac{I_{GATE}}{C1} \text{ or } \frac{I_{LIMIT(5VOUT)} - I_{LOAD(5VOUT)}}{C_{LOAD(5VOUT)}} \text{ or } = \frac{I_{ILIMIT(3.3VOUT)} - I_{LOAD(3.3VOUT)}}{C_{LOAD(3.3VOUT)}} \quad (5)$$

whichever is slowest. The power-up time for the 5V or 3.3V outputs where the inrush current is constrained by the LTC1644's foldback current limit can be approximated as:

$$t_{ON(VOUT)} < \frac{2 \bullet C_{LOAD} \bullet V_{OUT}}{I_{LIMIT(MINVOUT)} - I_{LOAD(MAXVOUT)}} \quad (6)$$

Note that Equation 6 can also be used to estimate the power-up times for the 12V and –12V outputs.

If the value of C1 is large enough that it alone determines the output voltage ramp rate, then the magnitude of the inrush current is:

$$I_{INRUSH(VOUT)} = \frac{C_{LOAD(VOUT)}}{C1 \bullet I_{GATE}} \quad (7)$$

The maximum power-up time for this condition can be approximated by:

$$t_{ON(VOUT)} < \frac{\left(V_{OUT} + V_{th(MAXMOSFET)}\right) \bullet C1}{I_{GATE(MIN)}} \quad (8)$$

where $V_{th(MAXMOSFET)}$ is the maximum threshold voltage of the external 5V or 3.3V MOSFET.

In general, the edge rate (dI/dt) at which the back-end 5V and 3.3V supply currents are turned on can be limited by increasing the size of C1. Applications that are sensitive to the edge rate should characterize how varying the size of C1 reduces dI/dt for the external MOSFET selected for a particular design.

In the event of a short circuit or overcurrent condition, the LTC1644's GATE pin can be pulled down within 2µs since a 1k (R5 in Figure 1) decouples C1 from the gates of the external MOSFETs (Q1 and Q2 in Figure 1).

TIMER Pin Capacitor Selection

The LTC1644 uses its TIMER pin to inhibit the circuit breaker function for a period of time after the OFF/$\overline{ON}$ pin is asserted low. This feature allows the part to power up large capacitive loads using its foldback current limit. The TIMER inhibit period can be expressed as:

$$t_{TIMER} = C_{TIMER} \bullet \frac{12V_{IN} - V_{TIMER}}{I_{TIMER}} \quad (9)$$

The timer period should be set longer than the duration of any inrush current that exceeds the LTC1644's foldback current limit, but yet be short enough not to exceed the maximum safe operating area of the 5V and 3.3V pass transistors in the event of a short circuit.

Reducing Inrush Current dI/dt

For applications that power up in current limit, where I_{INRUSH} is determined by the LTC1644's foldback current limit instead of Equation 7, the circuit shown in Figure 3 can be used to limit the dI/dt. The circuit uses TIMER pin source-follower Q3 and the voltage divider created by R6 and R7 to create a time-dependent offset voltage that is subtracted from the voltage being regulated across the 5V sense resistor R2 by the LTC1644. As the TIMER pin voltage increases, the voltage being regulated across the sense resistor offset voltage crosses through zero and the 5V supply current begins to ramp up in a linear manner (see Figure 4). TIMER pin source-follower Q4 inhibits the positive feedback from the LTC1644's 5V foldback current limit thus preventing the dI/dt rate from exceeding 1.5A/ms as V_{5VOUT} begins to ramp up from 0V. After the TIMER pin voltage has ramped to its final value, Q4 becomes linear and the LTC1644's $5V_{OUT}$ pin is connected to the back-end 5V supply. Since the GATE pin is common to both the 5V and 3.3V external MOSFETs, the 3.3V supply current will track the 5V supply current if Q1 and Q2 are matched. Applications that require an active pull-down to discharge the 5V load capacitance will need to add an additional N-channel transistor (drain tied to the back-end 5V power plane, source tied to ground and gate tied to the BD_SEL# signal) since the LTC1644's $5V_{OUT}$ pin is disconnected from the load when the BD_SEL# is deasserted.

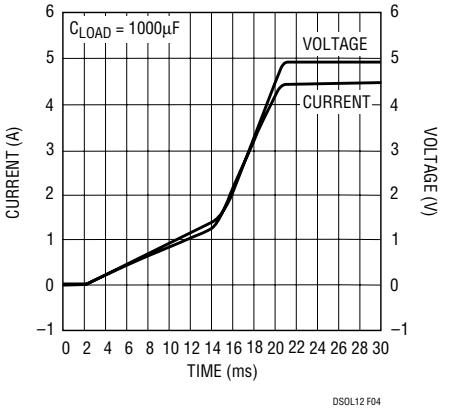

Figure 4. 5V dI/dt Auxiliary Control Circuit Power-Up Waveforms

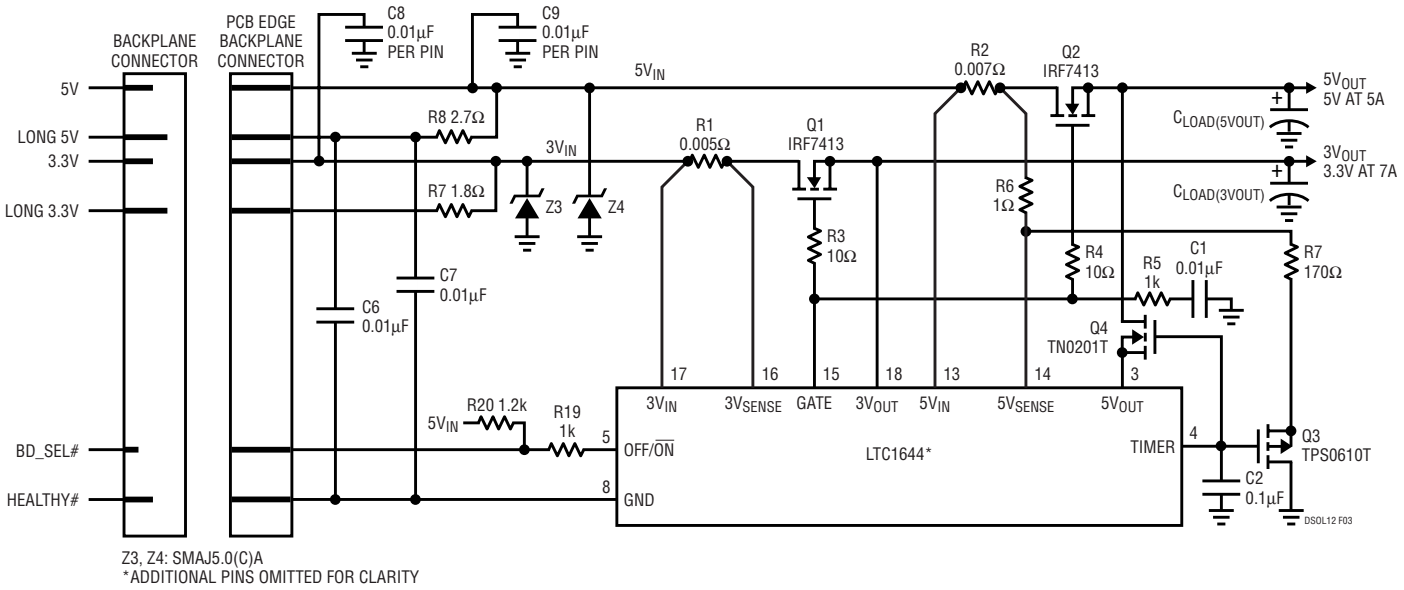

Figure 3. 5V and 3.3V dI/dt Control Circuit

Design Example

As a design example, consider a CompactPCI Hot Swap control application with the following power supply requirements:

Table 1. Design Example Power Supply Requirements

Voltage Supply	Maximum Supply Current	Load Capacitance
12V	500mA	100µF
5V	5A	2000µF
3.3V	7A	2000µF
–12V	100mA	100µF

The first step is to select the appropriate values of R_{SENSE} for the 5V and 3.3V supplies. Calculating the value of R_{SENSE} is based on $I_{LOAD(MAX)}$ and the lower limit for the circuit breaker threshold voltage (40mV for both the 5V and 3.3V circuit breakers). If a 1% tolerance is assumed for the sense resistors, then 5mΩ and 7mΩ resistor values yield the following minimum and maximum I_{TRIP} values:

Table 2. I_{TRIP} vs R_{SENSE}

R_{SENSE} (1% R_{TOL})	$I_{TRIP(MIN)}$	$I_{TRIP(MAX)}$
5mΩ	7.9A	14.1A
7mΩ	5.7A	10.1A

The second step is to select MOSFETs for the 5V and 3.3V supplies. The IRF7457's on resistance is less than 10.5mΩ for V_{GS} > 4.5V and a junction temperature of 25°C. Since the maximum load current requirement for the 3.3V supply is 7A, the steady-state power the device may be forced to dissipate is 514mW. The IRF7457 has a junction-to-ambient thermal resistance of 50°C/W. If a maximum ambient temperature of 50°C is assumed, this yields a junction temperature of 75.7°C. According to the IRF7457's Normalized On-Resistance vs Junction Temperature curve, the device's on-resistance can be expected to increase by about 20% over its room temperature value. Recalculation of the steady-state values of R_{ON} and junction temperature yields approximately 12.6mΩ and 81°C, respectively. The I • R drop across the 3.3V sense resistor and series MOSFET at max load under these conditions will be 123mV.

The next step is to select appropriate values for C1 and C_{TIMER}. Assuming that the total current for the 5V supply is constrained to less than 6A during power-up (six 5V medium length connector pins at 1A per pin), then the inrush current shouldn't exceed:

$$I_{INRUSH} < 6A - I_{LOAD(5VOUT)} = 6A - 5A = 1A$$

This yields:

$$C1 > \frac{I_{GATE(MAX)} \bullet 2000\mu F}{I_{INRUSH(MAX)}} = \frac{100\mu A \bullet 2000\mu F}{1A} = 200nF$$

Hence a C1 value of 220nF ±10% should suffice. The value of C_{TIMER} for this design example will be constrained by the duration of the 12V supply inrush current, which according to Equation 6 is:

$$t_{ON(12VOUT)} < \frac{2 \bullet C_{LOAD} \bullet 12V}{I_{LIMIT(MIN)} - I_{LOAD(MAX)}}$$
$$= \frac{2 \bullet 100\mu F \bullet 12V}{525mA - 500mA} = 96ms$$

In order to guarantee that the LTC1644's TIMER fault inhibit period is greater than 96ms, the value of C_{TIMER} should be:

$$C_{TIMER} > \frac{96ms \bullet I_{TIMER(MAX)}}{12V - V_{TIMER(MAX)}}$$
$$= \frac{96ms \bullet 27\mu A}{12V - 1.3V} = 242nF$$

So a value of 330nF ±10% should suffice.

The next step is to verify that the thermal ratings of the external 5V and 3.3V MOSFETs aren't being exceeded during power-up cycles into the designed loads or into a short circuit. The power dissipated by the 5V MOSFET during a normal power-cycle is given by Equation 3 as:

$$P_{OFF\text{-}ON(5V)} < \frac{5V \bullet (1A + 5A)}{2} = 15W$$

The duration of this power-pulse is given by Equation 4 as:

$$t_{INRUSH(5V)} = \frac{2000\mu F \bullet 5V}{1A} = 10ms$$

The IRF7457 data sheet's Maximum Effective Thermal Response vs Pulse Duration curve reveals that the MOSFET's junction-to-ambient temperature can be expected to increase no more than 30°C during the power-up cycle. A similar analysis of the 3.3V MOSFET reveals that it will experience less than a 20°C increase in junction-to-ambient temperature during power-up into the designed load.

The duration and magnitude of the power pulse that results during a short-circuit condition on either the 5V or 3.3V outputs is a function of the TIMER capacitor and the LTC1644's foldback current limit. In the case of a hard-short on the 5V supply, the maximum amount of power dissipated in the external MOSFET is:

$$P_{SHORTCIRCUIT(MAX)} < \frac{5V \bullet V_{FB(MAX)}}{R_{SENSE}}$$
$$= \frac{5V \bullet 15mV}{7m\Omega} = 10.8W$$

The maximum duration of the power-pulse is given by Equation 9 as:

$$t_{PULSE(MAX)} < C_{TIMER(MAX)} \bullet \frac{12V - V_{TIMER(MIN)}}{I_{TIMER(MIN)}}$$
$$= \frac{(330nF + 33nF) \bullet (12V - 0.5V)}{15\mu A} = 276ms$$

The IRF7457's Maximum Effective Thermal Response vs Pulse Duration curve indicates that the increase in junction-to-ambient temperature during a power cycle into the $5V_{OUT}$ short circuit will be less than 87°C. A similar analysis of the 3.3V IRF7457 MOSFET reveals that the increase in its junction-to-ambient temperature resulting from a $3V_{OUT}$ short-circuit will be less than 80°C.

Conclusion

Using the LTC1644, a CompactPCI board can be made such that system power can remain on when the board is inserted or removed. With careful attention to component selection, the LTC1644 offers an effective solution for a wide range of CompactPCI Hot Swap control applications.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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